REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-19 are pending in this application. Claims 1, 2, 6, 8, 9, 14, 16, and 17 are amended and Claim 19 is added by the present amendment.

Amendments to the claims and new Clam 19 find support in the application as originally filed, at least in the originally filed claims. Thus, no new matter is added.

In the outstanding Office Action, Claims 2, 6, 8, 9, and 11-18 were rejected under 35 U.S.C. § 112, second paragraph; Claims 1, 3, and 10 were rejected under 35 U.S.C. § 102(b) as anticipated by Japanese Patent Publication 08-205539 to Yoshikawa; Claims 4-6 and 8 were rejected under 35 U.S.C. § 103(a) as unpatentable over Yoshikawa in view of U.S. Publication 2003/0222627 to Hwang; Claims 2, 11, and 18 were rejected under 35 U.S.C. § 103(a) as unpatentable over Yoshikawa in view of U.S. Publication 2004/0113596 to Peron; Claims 12-14, 16, and 17 were rejected under 35 U.S.C. § 103(a) as unpatentable over Yoshikawa in view of Peron and Hwang; and Claims 7 and 15 were rejected under 35 U.S.C. § 103(a) as unpatentable over Yoshikawa in view of Peron and Japanese Patent Publication 10-174428 to Chinomi et al. (herein "Chinomi").

Regarding the rejections under 35 U.S.C. § 112, second paragraph, Claim 2 is amended to remove the term "loosely", and Claims 6, 8, 9, 14, 16, and 17 are amended to recite the claimed features in light of comments in the Office Action. Accordingly, it is respectfully requested the rejections under 35 U.S.C. § 112, second paragraph, be withdrawn.

Further, Applicants respectfully traverse the rejection of Claims 1, 3, and 10 under 35 U.S.C. § 102(b) as anticipated by Yoshikawa.

Claim 1 is directed to a power factor improving circuit that includes, in part, a main switch and a control section. The control section controls a switching frequency of the main switch based on a current flow. Independent Claim 2 includes similar features.

In a non-limiting embodiment, Applicants' Figure 5 shows an example of a power factor improving circuit including a control circuit 10 having a voltage controlled oscillator 115 which produces a triangle wave signal that is supplied to a pulse width modulator (PWM) comparator 116. The voltage controlled oscillator 115 receives a voltage signal from the node connecting a negative side output terminal P2 of a full-wave rectifier B1 and a current sensing resistor R, and accordingly, the received voltage signal varies with the amount of current flowing through the resistor R. Thus, in this example, voltage controlled oscillator 115 varies ***a frequency*** of the produced triangle wave signal based on the amount of current flowing through resistor R (e.g., current flowing into the rectifier circuit). Further, the pulse-width modulator comparator 116 controls ***a duty cycle*** (i.e., a ratio of portion of a clock period during which the main switch is on to a portion of the clock period when the main switch is off) of the on/off signal supplied to the gate of the main switch Q1. In particular, the pulse-width modulator comparator 116 controls the switch duty cycle based on i) a difference between the output voltage at RL and a desired voltage E1 produced by error amplifier 111, and ii) the variable frequency signal produced by the voltage controlled oscillator 115. In other words, the control circuit 10 controls both the switching duty cycle and the switching frequency of the main switch, based on a sensed current.

As discovered by the Applicants, by controlling both the duty cycle and frequency of the main switch, and in particular by decreasing a switching frequency at a portion of an AC cycle when an input current is low, it is possible to improve miniaturization, efficiency, and to reduce noise produced by a power factor improving circuit.[1]

[1] Specification at paragraphs [0015] and [0020].

Applicants respectfully submit that Yoshikawa fails to teach or suggest each of the features of the independent claims. For example, it is respectfully submitted that Yoshikawa fails to describe or otherwise suggest a power factor improving circuit with a portion that controls a switching frequency of a main switch. Further, Applicants respectfully traverse the assertion in the Office Action that Yoshikawa discloses that feature in Yoshikawa's Fig. 1, reference R1 and G, or at paragraphs 16-19.[2]

Yoshikawa indicates that a converter includes a transistor Q1, a resistor R, and a SIN following circuit 3.[3] Further, Yoshikawa indicates that the SIN following circuit 3 outputs an on-off signal L for turning on and off the transistor "in such a manner that the input current of the diode bridge becomes nearly the sine wave in response to input voltage waveform."[4] Further, as evidenced by Yoshikawa drawing 2, lines (D) and (E), drawing 5, lines (a)-(d), drawing 7, lines (a)-(c), drawing 3, lines (G)-(M), and drawing 4, lines (G)-(M), each embodiment according to Yoshikawa includes signals having a fixed frequency (e.g., fixed switching frequency) and variable duty cycle (e.g., variable switching duty cycle). Moreover, in the paragraphs of Yoshikawa cited in the Office Action, Yoshikawa indicates that a pulse oscillator circuit 35 outputs a ***constant frequency*** pulse K (shown in drawing 3 (K) and drawing 4 (K), sets a latch circuit 36 by falling of the constant frequency pulse K, and makes on-off-signal L H level, and the transistor Q1 is turned on/off by the L H level.[5] Thus, according to Yoshikawa, the switch Q1 (e.g., main switch) has a fixed switching frequency.

In other words, the converter of Yoshikawa appears only to control a switching ***duty cycle*** of a main switch, and Yoshikawa does not appear to control a ***switching frequency*** of the main switch. Accordingly, Applicants respectfully submit that Yoshikawa fails to teach

[2] Office Action at page 3, numbered paragraph 4.
[3] Yoshikawa at Abstract and drawing 1.
[4] Yoshikawa at Abstract.
[5] Yoshikawa at paragraph [0016] (emphasis added).

or suggest "a control section which . . . controls a switching frequency of the main switch," as recited in independent Claims 1 and 2.

Further, Applicants respectfully traverse the assertion in the Office Action that Yoshikawa teaches the voltage varying section of Claim 10.

Applicants' Figure 21 shows a non-limiting example of a voltage varying section 12 that inputs an output fed back from the current detection amplifying section 13 and the error voltage signal from the error voltage generating section 11.

In contrast, in the voltage varying section 33 of Yoshikawa Fig. 1, a signal from a DC voltage PI control circuit 32 according to the error voltage signal is inputted. However, according to Yoshikawa, an output fed back from a current detection amplifying section CPI is not inputted. Accordingly, the voltage varying section of Claim 10 is different from the voltage varying section of Yoshikawa.

Accordingly, Applicants respectfully submit that independent Claims 1 and 2, and claims depending therefrom, patentably define over Yoshikawa.

Thus, it is respectfully requested the rejection of Claims 1, 3, and 10 under 35 U.S.C. § 102(b) as anticipated by Yoshikawa be withdrawn.

Further, Applicants respectfully traverse the rejections of Claims 2, 4-9, and 11-18 under 35 U.S.C. § 103(a) as unpatentable over Yoshikawa in view of Hwang, Peron, and/or Chinomi, with respect to amended independent Claims 1 and 2.

Amended independent Claim 2 is directed to a power factor improving circuit that includes, in part, a main switch and a control section. The control section controls a switching frequency and a switching duty cycle of the main switch. Amended independent Claim 1 includes similar features.

Applicants respectfully submit that Yoshikawa, Hwang, Peron, and Chinomi, whether taken individually or in combination, fail to teach or suggest each of the features of each of

the amended independent claims. For example, it is respectfully submitted that those references fail to teach a control section that controls a switching frequency ***and*** a switching duty cycle of a main switch.

As discussed above, Yoshikawa only suggests that a control section controls a switching duty cycle of a main switch.

Hwang describes a power factor correction circuit in which an output voltage is monitored to form a carrier signal that "is compared to a signal that is representative of the input current ***to control the switching duty cycle***."[6] In addition, Hwang indicates that "a signal representative of the input voltage is summed with the signal that is representative of the input current, or with the carrier signal, in order to effectively ***control the switching duty cycle*** under light load conditions and conditions in which the input voltage can vary."[7] Moreover, Hwang indicates that an error signal may be used to "***affect the duty cycle of the switches*** SW1 and SW2."[8] Further, Hwang indicates that

> ***the duty cycle of the switches SW1 and SW2 is controlled*** with negative feedback to maintain the input current Iin in phase with the input voltage Vin and to regulate the output voltage Vout. It will be apparent that leading or trailing edge modulation techniques may be utilized and that other types of modulation may be used, such as frequency modulation.[9]

In other words, Hwang indicates that a duty cycle of a switch SW1 or SW2 (e.g., a main switch) is controlled using negative feedback, a leading or trailing edge modulation technique, or frequency modulation. Hwang also indicates that "the level of power is controlled by controlling the timing of opening and closing the switches SW1 and SW2, such as by pulse-width modulation ***or*** frequency modulation."[10] Thus, Hwang only describes controlling a duty cycle (e.g., switching duty cycle) of a main switch, or in particular the timing of the rising and falling edges (e.g., duty cycle) according to a pulse-width modulation

[6] Hwang at Abstract (emphasis added).
[7] Hwang at Abstract (emphasis added).
[8] Hwang at paragraph [0041] (emphasis added).
[9] Hwang at paragraph [0057] (emphasis added).
[10] Hwang at paragraph [0038] (emphasis added).

or a frequency modulation technique, and Hwang does not appear to imply or suggest controlling a switching frequency of the main switch.

Further, even if one were to incorrectly conclude that the "frequency modulation" of Hwang implies a method of varying a frequency of the main switch, it would not be possible to conclude that Hwang suggests a method of controlling both the switching duty cycle ***and*** switching frequency of the main switch, because Hwang merely indicates that pulse-width modulation and frequency modulation are alternatives (i.e., Hwang indicates controlling the switch timing by "pulse-width modulation ***or*** frequency modulation"[11]) and does not teach or suggest performing ***both*** switching duty cycle control ***and*** switching frequency control for any purpose, and it is believed that Hwang provides no motivation for one of skill in the art to have combined those approaches.

Thus, it is respectfully submitted that Hwang fails to supply or suggest the claimed features lacking in Yoshikawa.

Peron describes an auxiliary switching circuit for a chopping converter including plural inductors and diodes to transfer a flow of energy. In particular, FIG. 5 of Peron shows a main winding L0, a primary winding L1, a second winding L2, a feedback winding L, and a diode D1. However, Peron fails to teach or suggest controlling a switching frequency and controlling a duty cycle of a main switch.

On the other hand, an example of the present invention includes, a primary winding 5a and a feed back winding 5b including a leakage inductance more than a predetermined inductance value. However, the invention of Claim 2 does not require a primary winding L1 and a diode D1 of Peron.

[11] Hwang at paragraph [0038] (emphasis added).

Further, an inductance L of Peron is comparatively small. A recovery current flowing into a switch K in Peron Fig. 7c is reduced by the impedance of the inductance L and of the primary winding L1.

In contrast, in the present invention, the recovery current flowing into a switch Q1 is largely reduced by the leakage inductance more than the predetermined inductance value. Accordingly, the present invention does not include the primary winding L1 and the diode D1 of Peron. Therefore, a power factor improving circuit of the present invention is miniaturized and becomes less expensive. Thus, Peron fails to supply the features of independent Claims 1 and 2 lacking in the disclosures of Hwang at Yoshikawa.

Chinomi describes a power-factor-improvement circuit in which a clock frequency of a signal generator is varied to thereby vary a switching frequency of a current switching means 1 (e.g., main switch). However, Applicants respectfully submit that Chinomi also fails to teach or suggest any control of the pulse-width of the current switching means 1, and therefore, it is respectfully submitted that Chinomi also fails to teach or suggest a power factor improvement approach that controls ***both*** switching duty cycle ***and*** switching frequency of a main switch. Thus, it is believed that Chinomi also fails to supply the features of independent Claims 1 and 2 lacking in the disclosures of Peron, Hwang, and Yoshikawa.

Accordingly, Applicants respectfully submit that amended independent Claims 1 and 2, and claims depending therefrom, patentably define over the disclosures of Chinomi, Peron, Hwang, and Yoshikawa, whether taken individually or in combination.

Thus, it is respectfully requested the rejections of Claims 2, 4-9, and 11-18 under 35 U.S.C. § 103(a) as unpatentable over Yoshikawa in view of Hwang, Peron, and/or Chinomi also be withdrawn.

Accordingly, it is respectfully submitted that independent Claims 1 and 2, and claims depending therefrom, are allowable.

Consequently, in light of the above discussion and in view of the present amendment this application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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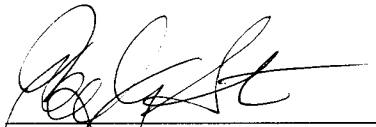

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